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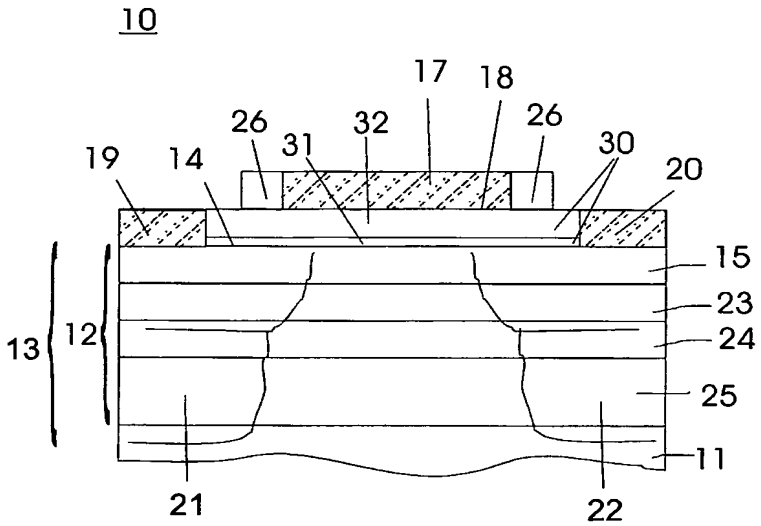
(54) Title: NITRIDE METAL OXIDE SEMICONDUCTOR INTEGRATED TRANSISTOR DEVICES



(57) Abstract: A self-aligned enhancement mode or depletion mode nitride based metal-oxide-compound semiconductor field effect transistor (10) includes a gate insulating structure comprised of a first oxide layer that in comprised of gallium oxides or indium oxides compounds (30) positioned immediately on top of the nitride compound semiconductor structure, and a second insulating layer comprised of either (a) oxygen and rare earth elements, (b) gallium oxygen and rare earth elements, or (c) gallium+indium and rare earth elements positioned immediately on top of said first layer. Together the lower indium oxide or gallium oxide layer and the second insulating layer form a epitaxial oxide gate insulating structure. The gate insulating structure and underlying compound semiconductor layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14) that is based on the nitride family of compound semiconductors. The first oxide layer serves to passivate and protect the underlying compound semiconductor surface from the second insulating layer and atmospheric contamination. A refractory metal gate electrode layer (17) is positioned on upper surface (18) of the second insulating layer. The refractory metal is stable on the second insulating layer at elevated temperature. Self-aligned source and drain areas, and source and drain contacts (19, 20) are positioned on the source and drain areas (21, 22) of the device. Multiple devices are then positioned in proximity and the appropriate interconnection metal layers and insulators are utilized in concert with other passive circuit elements to form an integrated circuit structure. Finally, NMOS and PMOS nitride based devices are positioned in proximity to for a complementary metal oxide semiconductor integrated circuit in nitride based compound semiconductors.

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